100 (new): A mass-produced solid state device comprising:

a solid state material substrate having a top surface; and

a defect-free solid state material layer no more than three atomic layers thick having at least one atomically smooth major surface, and positioned on the top surface of the substrate;

at least a central portion of the solid state material layer having a non-flat major surface uniformly contacting intimately onto at least a selected portion of the top surface of the solid state material substrate to avoid production problem due to excessive leakage current.

101 (new): A solid state device as in claim 100 in which the solid state material layer has at least two of the following features: a) having an atomically smooth bottom surface; b) having a curved top surface; c) having an atomically smooth bottom gate layer; d) made of a single strengthened material; e) accurate to one atomic layer in thickness; f) is of an aged device material g) is atomically fine-grained; h) has oriented grains; i) is stronger than uncontacted device material; and j) less than two atomic layers thick.

102 (new): A mass-produced solid state device comprising:

a solid state material substrate having a top surface; and

a defect-free solid state material layer no more than three atomic layers thick having at least one atomically smooth major surface, and positioned on the top surface of the substrate;

at least a central portion of the solid state material layer having a non-flat major surface uniformly contacting intimately onto at least a selected portion of the top surface of the solid state material substrate to avoid production problems due to excessive

leakage current, said solid state material substrate having a central portion of zero bottom width.

103 (new): The device as in claim 100 in which the solid state material layer has no flat area at its bottom, but has an accuracy of better than a single atom on a layer dimension selected from the group consisting of thickness, depth, curvature, shape, size, chemical composition profiling, and lateral location.

104 (new): The device as in claim 100 in which at least a portion of the solid state material layer is surfaced strengthened, whereby the uniformly intimately contacted solid state material layer is stronger than the uncontacted solid state material itself.

105 (new): The device as in claim 100 in which the solid state material layer is sufficiently thin and flexible so as to yield under stress preventing device failure.

106 (new): The device as in claim 100 in which the solid state material layer is of an aged or burned-in solid state material.

107 (new): The device as in claim 100 having a thickness of less than three atomic layers thereby forming a thin-film integrated circuit device.

108 (new): The device as in claim 100 wherein the solid state material layer has a curved major surface with a radius of curvature of less than 0.5 microns.

109 (new): The device as in claim 100 in which material of the solid state material layer is at least one order of magnitude purer than the solid state material prior to said uniformly intimate contacting.

110 (new): The device as in claim 100 in which the solid state material layer has an accuracy in thickness of on atomic layer.

111 (new): The device as in claim 100 in which the solid state material layer comprises an ion implanted region with a depth accurate to two atomic layers.

112 (new): A solid state device as in claim 100 including:

first and second solid state material pockets positioned adjacent to each other, but laterally separated by a gap, on the top surface of the substrate;

the solid state material layer filling and bridging the gap between the two adjacent solid state material pockets; and

at least a portion of the solid state material layer having an accuracy in thickness of better than two atomic layers.

113 (new): A solid state device as in claim 112 in which:

at least a part of the substrate is a semiconductor of a first conductivity type; and

at least one of the semiconductor pockets is of a second conductivity type forming at least one PN junction region where the part of the substrate contacts the at least one semiconductor material pocket.

114 (new): The device as in claim 100 in which the solid state material layer is selected from the group consisting of a single-material gate layer and a single-material field layer.

115 (new): The device as in claim 100 in which the substrate material is selected from the group consisting of Si, Ge, Si-Ge, InP, InSb, GaAs, SiC, InAs, superconductor, diamond, semiconductor material, intrinsic semiconductor material, substantially electrically insulating material, and substantially electrically conducting material, and mixture thereof.

116 (new): The device as in claim 100 selected from the group consisting of metal-oxide-semiconductor (MOS) device, conductor-insulator-semiconductor (CIS) device, thin-film integrated circuit, flexible integrated circuit, electro optical device, electrooptomagnetic devices and mixtures thereof.

117 (new): A mass-produced solid state device comprising:

a solid state material substrate having a top surface; and

a defect-free solid state material layer no more than three atomic layers thick having at least one atomically smooth major surface, and positioned on the top surface of the substrate;

at least a central portion of the solid state material layer having a non-flat major surface uniformly contacting intimately onto at least a selected portion of the top surface of the solid state material substrate to avoid production problems due to excessive leakage current, and including

first and second solid state material substrate pockets positioned adjacent to each other, but laterally separated by a gap, on top surface of the substrate;

the solid sate material layer filling and bridging the gap between the two adjacent solid state material pockets; and

at least a portion of the solid state material layer having an accuracy in thickness of better than two atomic layers; and in which:

the first and second solid state material substrate pockets are respectively source and drain semiconductor pockets in a solid state device and separated by a gap from each other;

the solid state material layer is an insulating gate layer filling and bridging the gap between the two pockets; and

the gate layer material has an atomically smooth surface on at least one of the top and bottom major surfaces thereof.

118 (new): A mass-produced solid state device comprising:

a solid state material substrate having a top surface; a defect-free solid state material layer no more than three atomic layers thick having at least one atomically smooth major surface, and positioned on the top surface of the substrate;

at least a central portion of the solid state material layer having a non-flat major surface uniformly contacting intimately onto at least a selected portion of the top surface of the solid state material substrate to avoid production problems due to excessive leakage current, and including

first and second solid state material pockets positioned adjacent to each other, but laterally separated by a gap, on the top surface of the substrate;

the solid sate material layer filling and bridging the gap between the two adjacent solid state material pockets; and

at least a portion of the solid state material layer having an accuracy in thickness of better than two atomic layers; and in which:

each of a major portion of the substrate, solid state material pockets, and solid state material layer consists essentially of a single semiconductor material doped to no more than 10 ppm of impurities whereby the device is made resistant to dynamic forces due to impacts, vibrations, and large and rapid accelerations and decelerations.

119 (new): The device as in claim 100 including a PN junction region having a curved adjoining surface without any flat bottom thereon, and contacting the substrate to thereby reduce but not eliminate at least one of thermal mismatch stress and volume change strain;

the remaining residual strain and stress on the curved adjoining surface of the PN junction region improving a selected device performance.

120 (new): The device as in claim 113 in which:

the at least one PN junction region has a curved adjoining surface without a flat portion thereon and;

the at least one of the first and the second solid state material pockets meets the curved adjoining portion of the at least one PN junction region.

121 (new): The device as in claim 100 in which the solid state material layer is an electrically insulating, curved field layer containing a substance selected from the group consisting of oxygen and nitrogen.

122 (new): A mass produced solid sate device comprising:

a solid state material substrate having a top surface; and

a defect-free solid state material layer no more than three atomic layers thick having at least one atomically smooth major surface, and positioned on the top surface of the substrate;

at least a central portion of the solid state material layer having a non-flat major surface uniformly contacting intimately onto at least a selected portion of the top surface of the solid state material substrate to avoid production problems due to excessive leakage current, and including

first and second solid state material pockets positioned adjacent to each other, but laterally separated by a gap, on the top surface of the substrate;

the solid sate material layer filling and bridging the gap between the two adjacent solid state material pockets; and

at least a portion of the solid state material layer having an accuracy in thickness of better than two atomic layers; and in which:

the first and second solid state material pockets are respectively source and drain semiconductor pockets in a solid state device; and

the solid state material layer is a single-material gate layer; and including:

a conductive gate electrode of an electrically conducting material positioned on th gate lay r to control flow of electronic carri rs from th source to the drain.

123 (new): A mass-produced solid state device comprising:

a solid state material substrate having a top surface; and

a defect-free solid state material layer no more than three atomic layers thick having at least one atomically smooth major surface, and positioned on the top surface of the substrate;

at least a central portion of the solid state material layer having a non-flat major surface uniformly contacting intimately onto at least a selected portion of the top surface of the solid state material substrate to avoid production problems due to excessive leakage current, and including:

first and second solid state material pockets positioned adjacent to each other, but laterally separated by a gap, on top surface of the substrate;

the solid sate material layer filling and bridging the gap between the two adjacent solid state material pockets; and

at least a portion of the solid state material layer having an accuracy in thickness of better than two atomic layers; and in which;

the first and second solid state material pockets are respectively source and drain semiconductor pockets in a solid state device; and

the solid state material layer is a single material gate layer; and

a conductive gate electrode of an electrically conducting material positioned on the gate layer o control flow of electronic carriers from the source to the drain;

the gate layer material is atomically smooth on at least one of top and bottom major surfaces thereof to achieve an exceptionally smooth and defect-free surface; and

material of the gate layer being purest at a bottom surface facing the substrate.

124 (new): The solid state device as in claim 100 in which:

the solid state material layer is a field layer separating and electrically isolating device components from each other on the substrate;

the field layer on a horizontal cross-section thereof has a plurality of curved sections; and

each curved section has an arc length defined by: l = r x A where l is the arc length, r is the radius of curvature of the arc, and A is the subtended arc angle;

each arc section being capable of flexing whereby the arc length is changed by delta l = r x delta A + A x delta r; and

the changes in delta l, delta r, and delta A all being in directions to reduce thermal mismatch strain and automatically stopping when the residual thermal mismatch strain is reduced by the changing arc length to a point such that the multiply curved field layer can tolerate without failure the residual thermal mismatch strain.

125 (new): The solid state device as in claim 100 in which the solid state material layer is curved to minimize thermal mismatch stresses.

126 (new): A mass-produced solid state device comprising:

a solid state material substrate;

at least one first solid state material pocket positioned on a first selected top surface of the substrate; and

a solid state material layer less than three atomic layers thick and having at least one atomically smooth but curved major surface which intimately contacts uniformly the first selected surface of the substrate onto a first specified portion of the at least one first solid state material pocket and in which the solid state material layer is curved and has a rounded bottom of zero width to minimize thermal mismatch stresses.

127 (new) A solid state device as in claim 126 in which the at least one atomically smooth but curved major surface intimately contacts uniformly, atom to atom, the first selected surface of the substrate onto said first specified portion of the at least one first solid state material pocket; and further comprising:

a second solid state material pocket positioned on a second selected surface of the substrate, and laterally adjacent to, but separated by a gap from, the at least one first solid state material pocket; and in which:

the solid state material layer fills the gap between the two solid state material pockets while intimately contacts uniformly with a second specified portion of the second solid state material pocket.

128 (new): A mass-produced solid state device comprising:

a solid state material substrate;

a left and a right adjacent solid state material pockets laterally separated by a gap and positioned on a common top surface of the substrate;

a curved solid state material layer which: a) is less than 40 angstroms thick; b) is positioned on the common top surface of the substrate to bridge the gap between the two solid state material pockets; c) has a rounded bottom; and d) is a single-material solid state material layer selected from the group consisting of gate layer and field layer.

129 (new): The solid sate device as claimed in claim 128 in which the solid sate state material layer is concavely curved when viewed from a top view.

130 (new): A mass-produced solid state device comprising:

a solid state material substrate;

at least a first solid state pocket positioned on a first selected top surface of the substrate; and

a solid state material layer less than three atomic layers thick and having at least one atomically smooth but curved major surface which intimately contacts uniformly the

first selected surface of the substrate onto a first specified portion of the at least one first solid state material pocket and in which:

the solid sate material layer is a single-material gate layer containing an ion-implanted substance selected from the group consisting of oxygen and nitrogen.

131 (new): A solid state material substrate having a top surface; and

a defect-free solid state material layer no more than three atomic layers thick having at least one atomically smooth major surface, and positioned on the top surface of the substrate;

at least a central portion of the solid state material layer having a non-flat major surface uniformly contacting intimately onto at least a selected portion of the top surface of the solid state material substrate to avoid production problems due to excessive leakage current, and including

first and second solid state material pockets positioned adjacent to each other, but laterally separated by a gap, on the top surface of the substrate;

the solid sate material layer filling and bridging the gap between the two adjacent solid state material pockets; and

at least a portion of the solid state material layer having an accuracy in thickness of better than two atomic layers; and in which;

at least a part of the substrate is a semi conductor of a first conductivity type;

said solid state material pockets are semiconductor material pockets;

at least one of the semiconductor pockets is a of a second conductivity type forming at least one PN junction region where the part of the substrate contacts the at last one semiconductor material pocket ; and the PN junction region has a depth of less than 70 nanometers.